A BROADBAND PASSIVE DELAY LINE STRUCTURE IN 0.18 MICRON CMOS FOR A GIGABIT FEED FORWARD EQUALIZER

A Thesis
Presented to
The Academic Faculty

By

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In Partial Fulfillment
Of the Requirements for the Degree
Master of Science in Electrical and Computer Engineering

Georgia Institute of Technology
December, 2004

A BROADBAND PASSIVE DELAY LINE STRUCTURE IN 0.18 MICRON CMOS FOR A GIGABIT FEED FORWARD EQUALIZER

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July 9, 2004

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ACKNOWLEDGEMENTS

I would like to thank my advisor Dr. Joy Laskar. In addition I would like to thank Dr. Edward Gebara for his guidance and Dr. Tentzeris and Dr. Papapolymerou for serving on my thesis reading committee. I would like to thank National Semiconductor for providing fabrication space.

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SUMMARY

A high-speed passive delay line structure for use in a Feed Forward Equalizer (FFE) implemented in a 0.18 micron CMOS process has been presented. Equalization is needed to achieve 20 Gbp/s data throughput after transmission through a 20 inch FR4 backplane channel. 4-PAM signaling and passive equalization are shown to be effective in recovering the transmitted signal. The FFE is implemented as an integrated FIR filter with gain blocks and delay elements. The delay element is implemented as an LC ladder structure. Electromagnetic simulations for inductor design are shown. A wideband inductor is fabricated and measurement results are compared to simulation results. A lumped element model for the inductor is presented. The delay line is designed and fabricated. Measurements results show performance at 10 GS/s. Recommendations for future work are presented.

CHAPTER 1

INTRODUCTION

1.1 Introduction and Problem Statement

The rapid growth of internet use in homes and businesses, corporate intranet use and the development of bandwidth hungry applications is fuelling the drive to develop solutions for multi-Gbps data transmission over wired channels such as coaxial cables, copper cables and PCB board traces. Furthermore, as optical networking technology moves toward 40 Gbps data rates, standard chip-to-chip, board-to-board, and server-to-server copper based interconnects which can provide up to few Gbps serial data transmission today pose a significant bottleneck to network speeds. Therefore, the development of serial data transmission solutions to support multi-Gbps (> 5 Gbps) data rates over copper channels is gaining importance.

High data rates over copper have usually been achieved using parallel streams of lower speed data. However, due to the increased cost and complexity associated with this technique, serial transmission over copper channels is receiving more attention (Infiniband, PCI Express, HSBI). Serial data transmission of multi-Gbps data over copper channels is challenged by the skin effect losses associated with copper, dielectric loss, and the associated noise components such as cross-talk noise. These losses induce inter-symbol interference (ISI), the effects of which worsen as data rates and the length of the

channel increases. Proposed solutions to meet these challenges include multilevel signaling, transmitter pre-emphasis, receiver equalization and cross-talk cancellation.

This project is based on a serial transmission solution for 20 Gbps throughput over a 20-inch backplane channel for future applications of board-to-board interconnections [1,2]. Specifically, the system used is a receiver equalizer employing a multilevel PAM 4 signaling technique and designed for serial data transmission over a 20-inch backplane channel. Measurements and system level simulations show that equalization is needed at the receiver in order to correctly receive a 20 Gbps PAM4 signal after a 20 inch FR4 channel [1,2]. A FIR filter topology that is composed of gain blocks and delay elements is chosen for this equalizer [1,2]. The delay element has to provide accurate time delay over the required bandwidth. Specifically, the design calls for an on chip high -speed accurate time delay structure. This thesis focuses on the design, fabrication and measurement of a high speed and accurate on-chip passive delay line structure. This includes system simulations, inductor design and modeling and on chip measurements of the inductor and delay line structures. The passive delay line investigated and fabricated for this thesis is part of a bigger system (FFE) and system simulations were carried on to include the parasitic contribution from the overall system

Chapter 2 presents background information on the problem, the signaling scheme used, equalizer system simulations and an introduction to passive delay lines. Chapter 3 is focused on inductor design and modeling. Chapter 4 focuses on the delay line results and measurements. Chapter 5 concludes with a summary and recommendations for future work.

CHAPTER 2

SYSTEM OVERVIEW

2.1 Background and System Description

A backplane is a printed circuit board used to connect daughter cards in a modular system. Figure 1 illustrates the basic structure of a backplane system. A standard channel consists of the backplane, connectors and daughter cards.

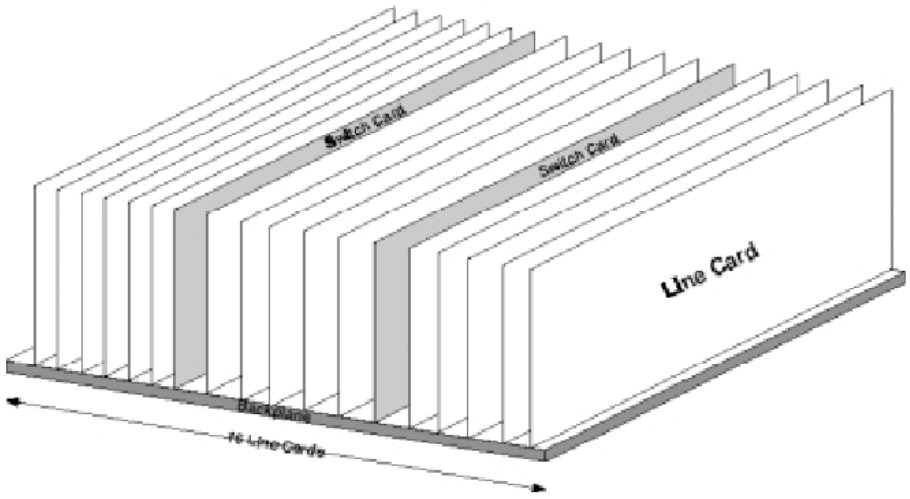

Fig. 1. Backplane with line cards.

Standard backplanes are made of commercial FR4 material, which has a frequency dependent loss characteristic like that of a low pass filter. Figure 2 shows the measured forward transmission of a 20-inch industry standard backplane with HMZD connectors. Differential forward transmission measurements using a standard network analyzer were carried out for 20 inch and 6 inch channels. The forward transmission of the 20 -inch backplane channel shows that the backplane is a band-limited channel with a 6 dB loss at about 1 GHz. This low pass characteristic of the channel causes the higher frequencies to be attenuated more severely than lower frequencies resulting in Inter-Symbol-Interference (ISI) in the time domain. Equalization is a process where the higher frequencies are boosted to extend the channel bandwidth and hence reducing ISI.

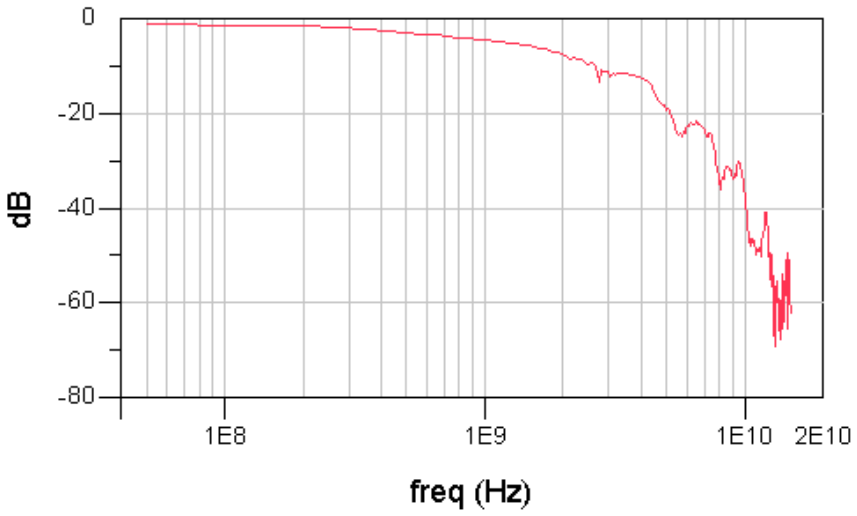

Fig. 2. 20-inch backplane forward transmission characteristic

Figures 3a and 3b shows the eye diagram of a 10 Gbps 4 PAM signal before and after the backplane [1]. As can be seen, equalization is needed to obtain the signal after the backplane. These plots are obtained from MATLAB simulations. The following section goes through the reasons for using 4 PAM signaling.

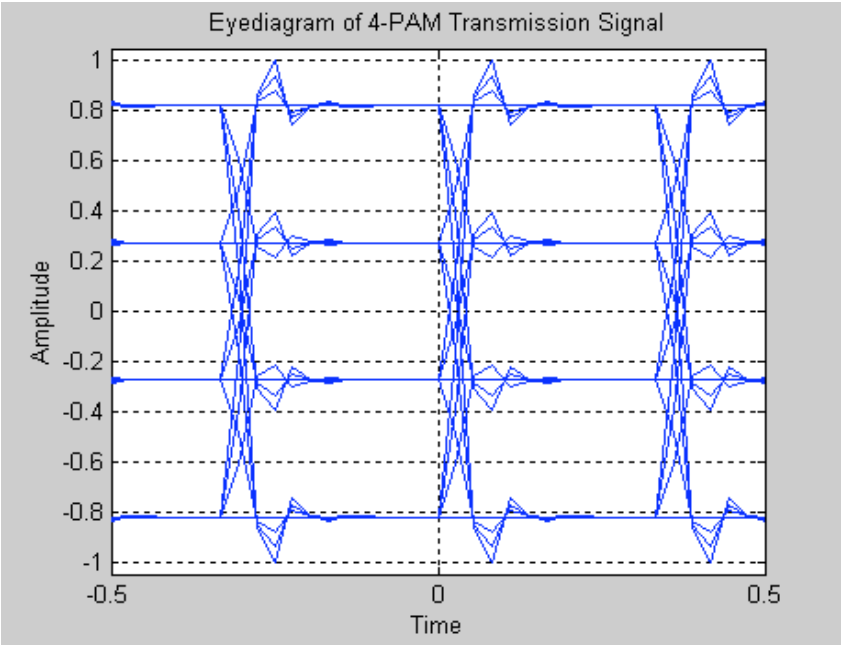

Fig. 3a. Eye diagram of a 4 PAM signal [1]

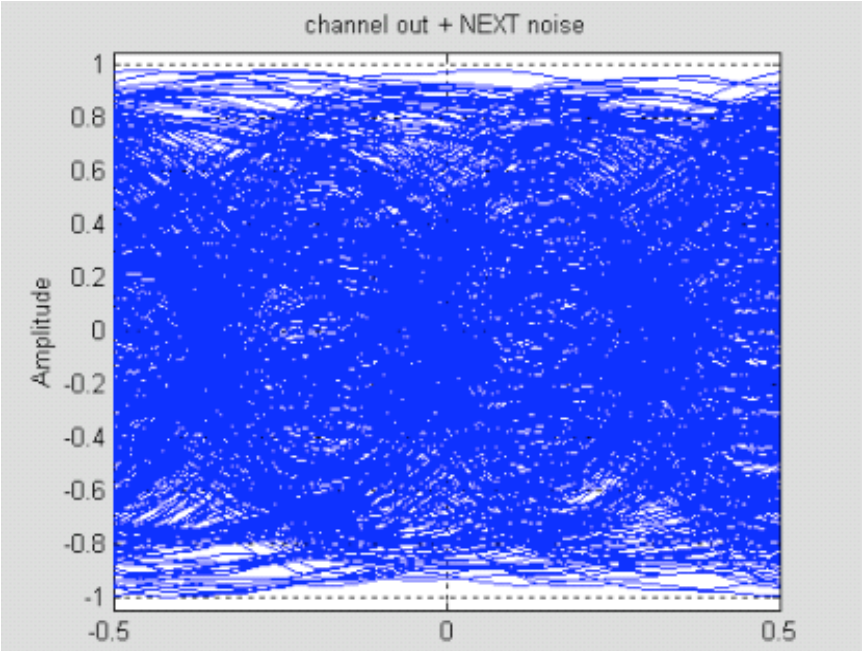

Fig. 3b. Eye diagram after passing through transfer function of the backplane channel [1]

2.2 Signaling scheme

The choice of signal to be sent over the backplane is an important one with implications on the performance as well as the complexity of the system. Traditionally, On-Off Keying (OOK) has been the choice for serial data transmission over copper. Recently, multilevel signaling has gained importance because of the advantage of reduced signal bandwidth that it offers. Transmission of multiple signal levels enables multiple bits per symbol resulting in a reduction in transmitted bandwidth for the same data rate. M- Pulse Amplitude Modulation (M-PAM) is a modulation scheme where different voltage levels signify different symbols. 4- Pulse Amplitude Modulation (4-PAM) is a multilevel modulation scheme 2 bits are encoded

into each amplitude level as opposed to one bit for OOK. This results in a smaller signal bandwidth for 4 PAM signals or in other words, a 4 PAM signal has double the data throughput than an OOK signal of the same bandwidth. 4 PAM and OOK are compared based on the frequency dependent characteristics of the forward transmission and Near-End Cross-Talk (NEXT) channel coupling for a 20-in FR-4 backplane shown in Figure 4 [1].

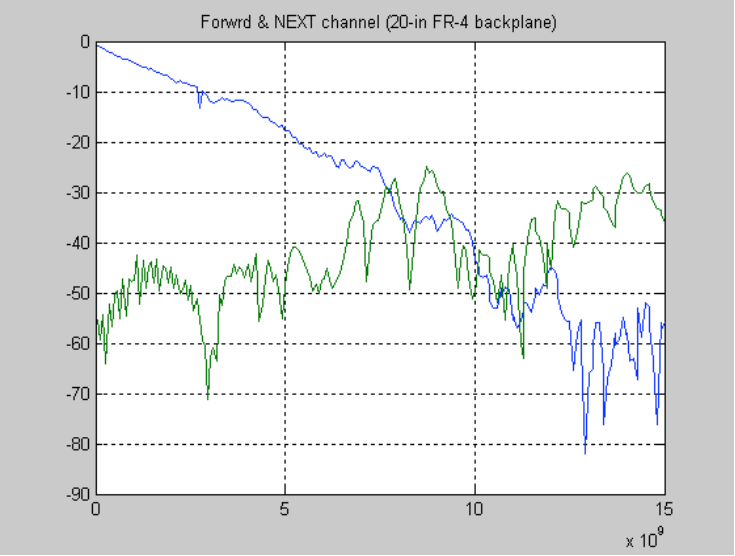

Fig. 4. Forward transmission and NEXT channel spectrum of 20-in FR4 backplane[1]

As data throughput increases over 1 Gbp/s, frequency dependent loss of the channel and Xtalk noise become major factors causing higher Bit Error Rate (BER) ($>10^{-12}$). As shown in Figure 4, the forward transmission decreases and the Xtalk increases with increasing frequency. 4-PAM signaling has a reduced signal bandwidth

and therefore experiences less channel loss and Xtalk noise compared to OOK, and hence less equalization is needed.

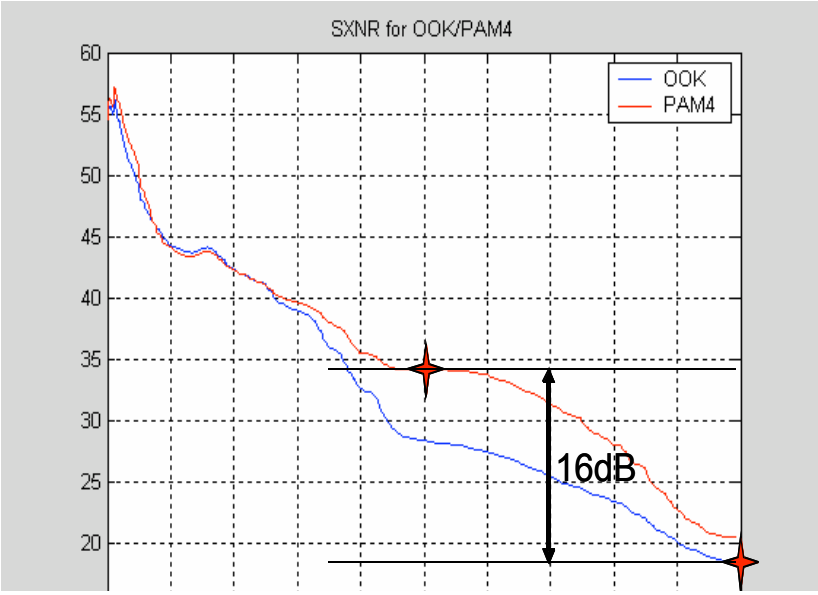

Fig. 5. SXNR curve for OOK and 4-PAM in 20-in FR-4 backplane channel [1]

As Xtalk noise is the dominant noise component for 20Gbps throughput data transmission, the Signal-to-Xtalk Noise Ratio (SXNR) is the figure of merit to determine the optimum signaling scheme. The SXNR for the data in Figure 4 is plotted in Figure 5. This figure shows the ratio of the victim signal Power Spectral Density (PSD) to the aggressor noise PSD as a function of frequency when OOK and 4-PAM signaling are used. Clearly, 4-PAM signaling has a better SXNR at higher data rates due to its higher spectral efficiency. When a data rate of 20Gbp/s is used the resulting SXNR values of OOK and 4-PAM signals are 27dB and 34dB, respectively. This translates in an overall SNR improvement of 7dB for 4-PAM, and therefore 4-

PAM was adopted as the signaling scheme for 20Gbp/s transmission over a 20-in backplane channel [1].

2.3 Passive Equalization

As mentioned earlier, equalization at the receiver side is needed to recover the transmitted signal after transmission through a 20-inch backplane channel. Transmitter equalizers have also been demonstrated in the literature. However, such a scheme would require a separate channel to communicate the tap information. For receiver equalization, a Decision Feedback Equalizer (DFE) and a Feed-Forward Equalizer (FFE) have been demonstrated in the literature as viable solutions for recovering the dispersed signal. A DFE combined with an FFE using 4-PAM signaling will result in an optimum solution. However, DFE implementation using 4-PAM signaling is very complex. Furthermore, it has been shown in system simulations that an FFE combined with 4-PAM signaling can equalize a 20 Gbp/s throughput 4-PAM signal [1]. An FFE with a Finite-Impulse Response (FIR) filter structure can be implemented in CMOS using innovative circuit techniques and is suitable for high –speed operation. Therefore, for this problem, an FFE FIR filter structure was chosen to equalize the received 4 PAM signal. Figure 6 shows the block diagram of a FIR filter structure [2]. System simulations performed in MATLAB show that optimum performance is achieved with a structure using 4 taps and each delay element having a delay of 33 picoseconds over the required bandwidth [1]. Figure 7 shows the received signal after equalization. [2].

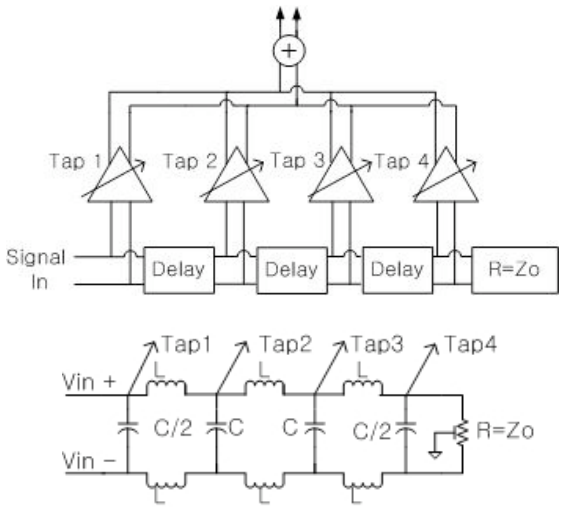

Fig. 6. Block diagram of a FIR filter structure

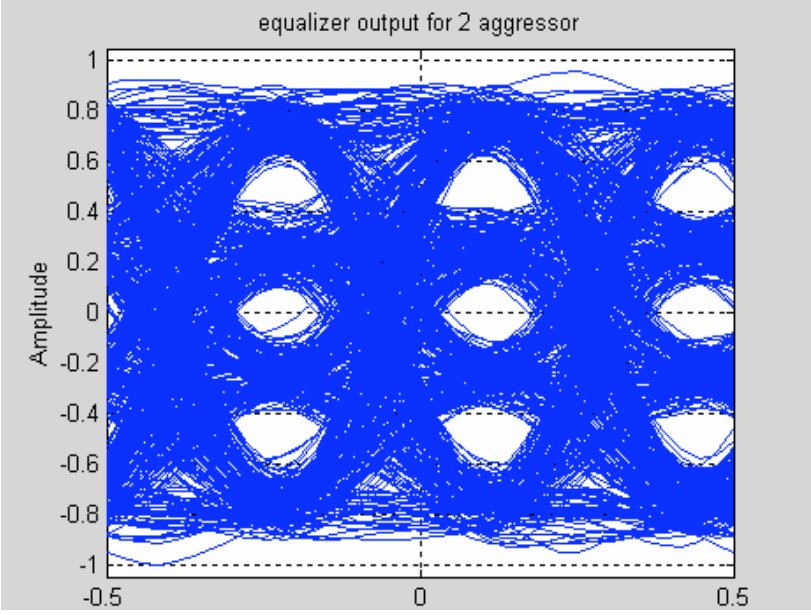

Fig. 7. Equalized PAM4 signal

2.4 Passive Delay lines

As mentioned earlier, a FIR filter structure is needed to equalize the signal after the backplane. A FIR filter structure consists of gain blocks and delay elements. The delay element has to provide accurate and constant time delay over the operating bandwidth. Artificial transmission line structures using inductors and capacitors have been used to time delay signals. Accurate time delay can be realized using an artificial transmission line structure using an LC ladder network [3]. A passive delay line is a low pass filter designed to delay or phase shift the input signal by a specific increment of time. From signal processing theory we know that delay in the time domain results in a phase shift in the frequency domain. Specifically, $t_d = -\frac{d(\arg(H(jw))}{dw}$. Therefore, for constant and accurate time delay over the operating bandwidth, a linear phase shift is required. Chapter 4 will provide a more in depth look at the design, fabrication and measurement of the passive delay line structure. The implementation of the delay line requires the use of wide-band inductors. Chapter 3 will focus on the design and fabrication of such a wideband inductor for use in the delay line.

CHAPTER 3

INDUCTOR DESIGN AND MODELING

3.1 Inductor Design

As mentioned in the previous section, wide band inductors are required for the delay line to provide accurate delay over the entire operating bandwidth. In order for the delay line to be integrated with the rest of the equalizer circuit, the inductor has to be fabricated on chip. On-chip inductors fabricated in silicon processes are commonplace in integrated circuits [4-11]. Most modern on-chip inductors are realized using a planar coil. Most modern processes provide one or more metal layers so single or multi layer spiral inductors can be fabricated on chip. The design process requires an accurate inductor model consisting of lumped elements for these spiral structures to be included in circuit simulations. Various compact equivalent lumped element circuit models for planar spiral inductors have been developed over the years [4-13]. The state-of-the-art models are developed by extracting the element values from measured data by means of some sort of parameter fitting process. The dependence of the inductor model on measurement data adds an extra step in the design cycle. Efficient integrated circuit design using inductors requires accurate modeling of the planar inductor structure prior to fabrication and measurements. Electromagnetic (EM) field solvers provide a way to accurately simulate the inductor structure before fabrication. THE EM simulator takes into account the substrate parasitics, the resistivity of the metal layers, and electromagnetic coupling with the surrounding environment. Several state-of-the-art commercial EM simulators such as

IE3D, ADS Momentum HP Ansoft, have been used to simulate planar inductor structures [4]. All of these tools use EM theory to simulate a given structure taking into account process parameters and device geometry. Any structure fabricated on a given process can thereby be simulated using such a simulator. The S parameters of the structure can be simulated and an accurate circuit model can be extracted using this simulated data.

The purpose of this chapter is to demonstrate the use of the IE3D EM simulator as a reliable tool for simulating planar inductor structures and to describe a compact circuit model for our spiral inductor that was used for delay line. The next section briefly describes the initial inductor design process.

3.2 Inductor EM simulations using IE3D

IE3D is an Electromagnetic Field simulator and Optimization software. IE3D's field solver is based on a full wave integral equation for solving the current distribution on 3D, multi-layer arbitrary structures.

For this thesis, National Semiconductor's 0.18 um 6 metal layer CMOS process was used. Figure 8 shows a simplified cross-section of the CMOS die.

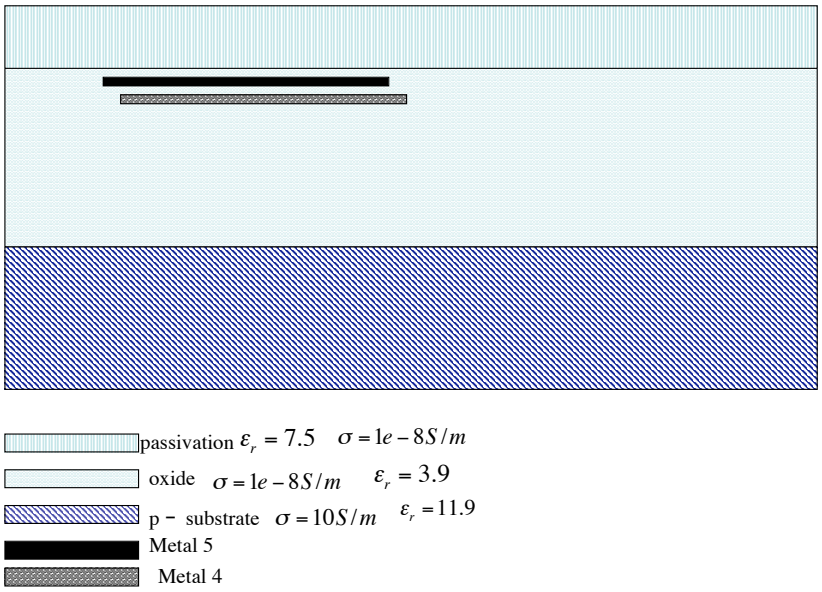

Fig. 8. Simplified cross-section of CMOS die

A 1.5 nH inductor over a 10 GHz bandwidth is required for the delay line. Figure 9 shows the structure of the spiral inductor.

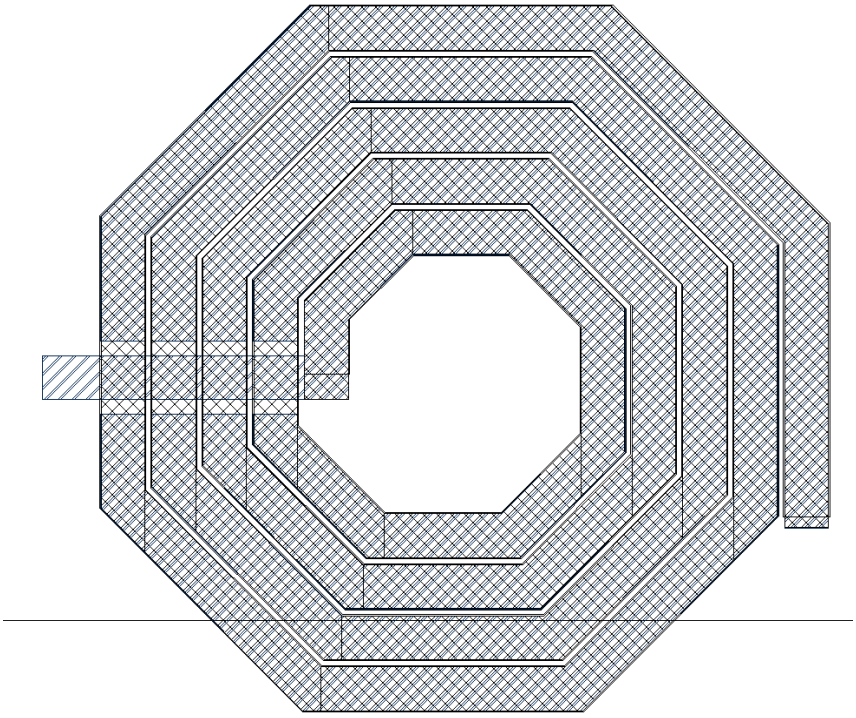

Fig.9. Spiral Inductor

The structure has 4.5 turns, the spiral inductor width is 6 um, the spacing between spirals is 1 um, and the spiral inductor diameter is 100 um. Metal 4 and metal 5 are stacked to form a double metal layer inductor. The two metal layers are connected using vias. The simulation takes into account the oxide, substrate, and metal layer conductivity and thickness, as well as the spiral geometry. The integrated circuit is measured with probes that connect to the circuit using signal and ground pads. These pads also contribute some parasitic effect to the measurement result. The effect of pad parasitics on inductor measurements has been well documented [5]. In order to simulate the effect of the pads on measurements results, the same spiral is simulated with signal pads to investigate the effect of the pads on the measured inductance. The resulting frequency response and extracted series inductance of the planar spiral with and without signal pads are shown in Figure 10. The plot shows that the pads have only a slight effect on the frequency response. The series inductance of the inductor was also extracted using the method shown in Section 3.4. Figure 11 shows the extracted inductance with and without the effect of the pad parasitics. It can be seen that the extracted inductance varies very little even with the effect of pad parasitics. This result will be corroborated by measurement results.

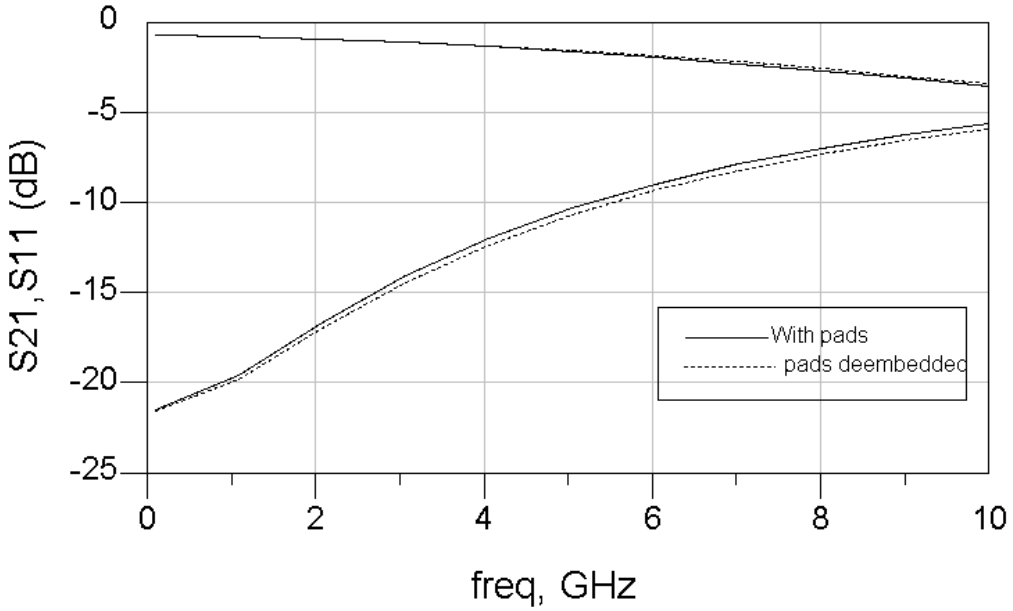

Fig.10. Simulated frequency response of spiral

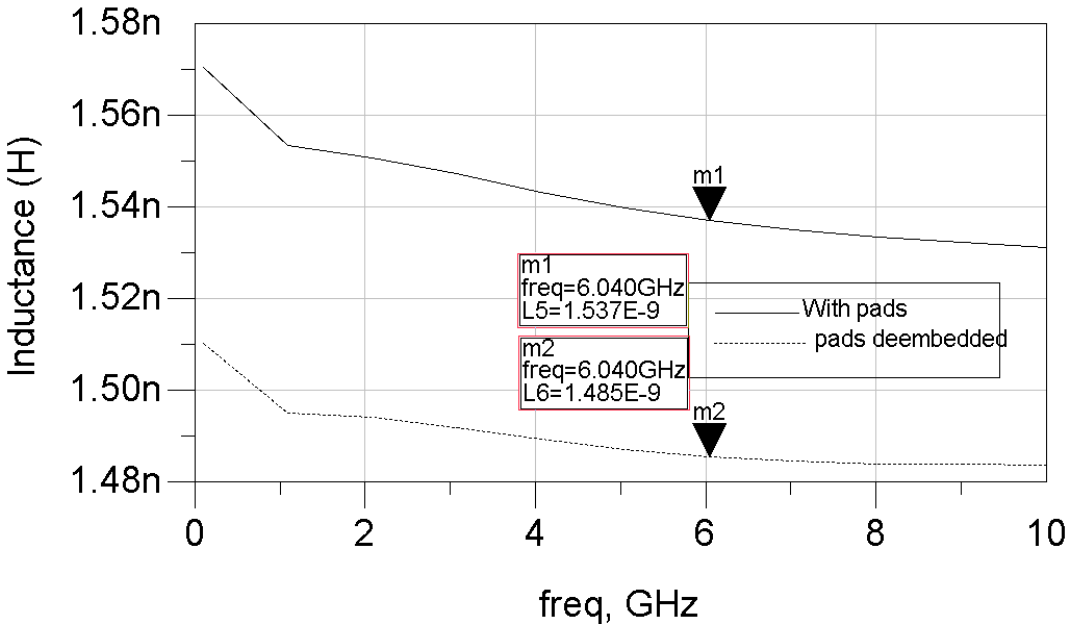

Fig.11. Series inductance of planar spiral

3.3 Inductor Layout and Measurements

The designed inductor is laid out using National Semiconductor's 0.18 um CMOS process. It has been shown that using stacked metal layers results in greater inductance for the same area compared to a single metal layers inductor [6]. Since the current flows through both metal layers in the same direction, the magnetic flux lines in the same direction result in higher mutual inductance. The inductor is laid out using metal 4 and metal 5 connected by several via structures. The spiral inductor needs to have input and output ports for measurement purposes. Therefore, a metal strip from the input port needs to overlap several turns to reach the inner turn of the spiral. This strip is referred to as the underpass. Metal 4 is used for the underpass.

It has been shown that the use of patterned ground shields (PGSs) can reduce substrate losses and significantly improve inductor Q values [7,8]. The inductor is laid out using a PGS between the inductor and the bulk substrate to reduce substrate losses. The on-chip pads can have an effect on the measured inductance especially at higher frequencies. Therefore, the effect of these pads needs to be extracted out of the measurement results. A dummy structure is also fabricated along with the inductor to extract out the effect of the pads. The dummy structure is an open structure, which can be used to measure the effect of the pads. Figure 12 shows the die photo of the laid out inductor structure with a dummy open structure to extract out pad parasitics. The effect of the pad parasitics was extracted using the method described in [6]. The S parameters were measured using the HP 8510C 2 port network analyzer from 0 – 10 GHz.

- The 2 port S parameters of the dummy structure, S_{pad} were measured.
- The 2 port S parameters of the inductor with pad $S_{inductor}$ were measured.

- The 2-port Y parameters, Y_{pad} were obtained from the S parameters using a matrix transformation.
- The two port Y parameters, $Y_{inductor}$ were obtained from the S parameters using a matrix transformation.
- The inductor Y parameters were obtained by subtracting Y_{pad} from $Y_{inductor}$
- The S parameters of just the inductor were obtained by converting the inductor Y parameters to S parameters again.

The measured frequency response of the structure before and after de-embedding was compared with EM simulations to prove the effectiveness of the EM simulator as a design tool. Figure 13a-b shows the comparison. The plots show that the frequency response of the structure is modeled quite accurately using the EM simulator. The simulated S11 after de-embedding varies by 2-3 dB from the measured S11. This discrepancy can be attributed to the probe positioning on the pads and coupling from the probes.

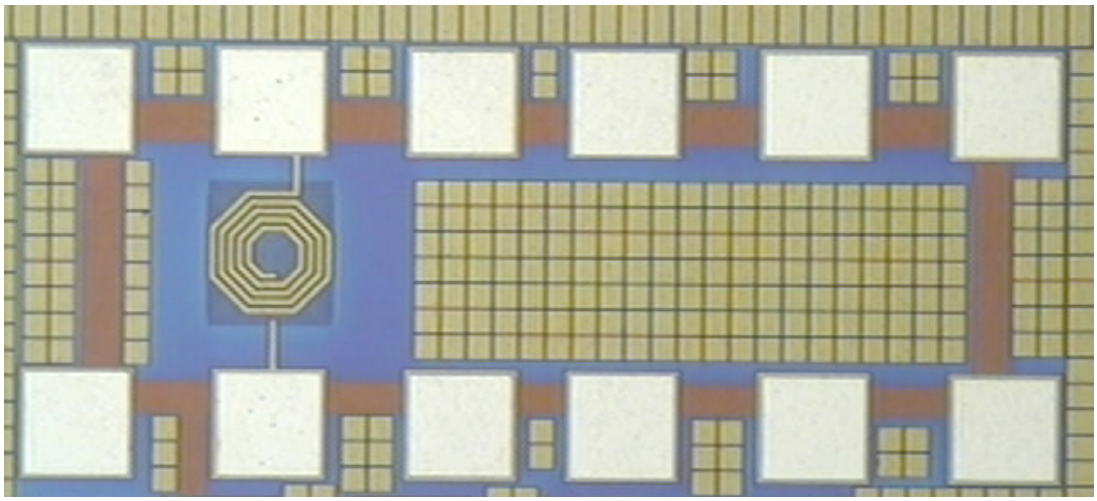

Fig. 12. Die photo of inductor and dummy structures

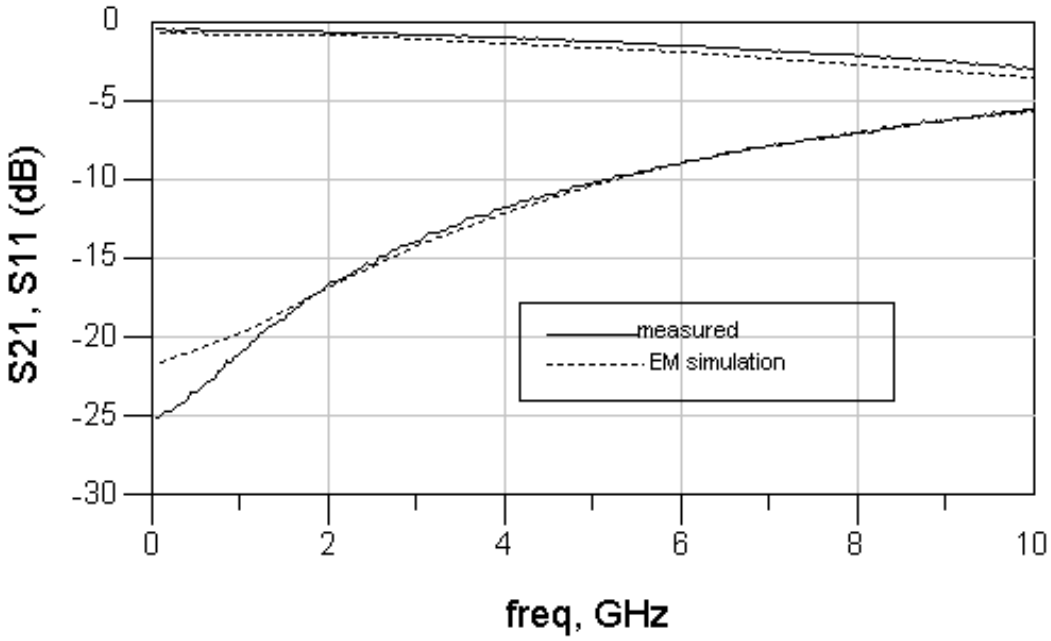

Fig. 13a. Frequency response of inductor structure before de-embedding

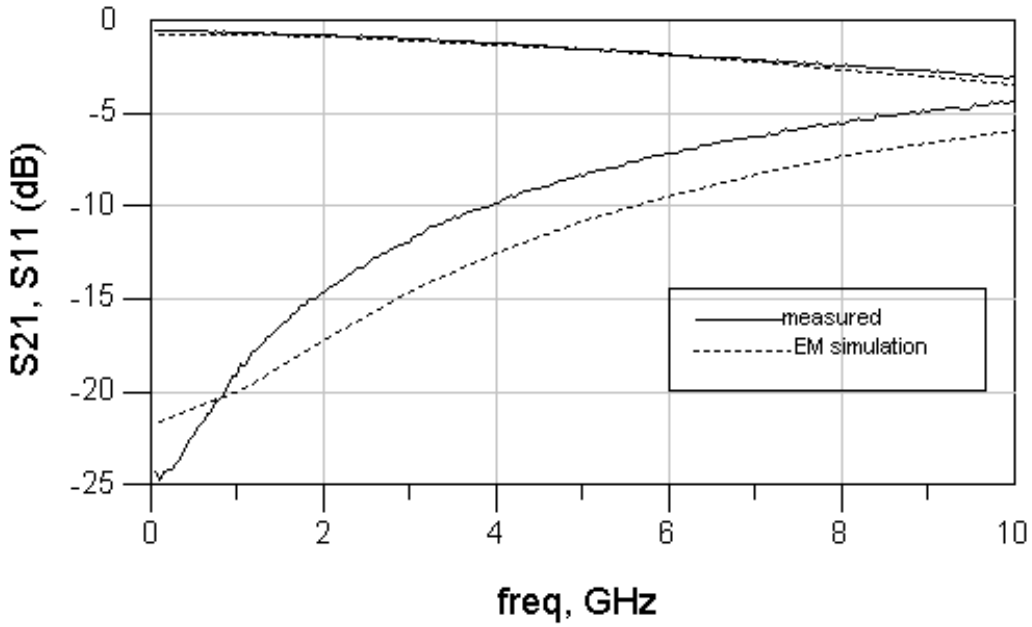

Fig. 13b. Frequency response of inductor structure after de-embedding

3.4 Inductance and Resistance

The 2 port S parameters of the inductor structure are measured and the pad parasitics de-embedded using the procedure outlined in the previous section. Y_{ind} is the two port Y parameters of the stand-alone inductor structure. The series impedance of the spiral can be calculated using (1)

$$Z_{serries}(\omega) = -\frac{1}{Y_{12}(\omega)} = R(\omega) + j\omega L(\omega) \qquad (1)$$

$$L(\omega) = \frac{imag(\frac{-1}{Y_{12}(\omega)})}{\omega} \qquad R(\omega) = real(Z(series(\omega)) \qquad (2)$$

The series inductance and resistance of a given spiral inductor is extracted from 2 port S parameters for measured, simulated and modeled inductors. Figure 14 shows the series inductance extracted from measured and de-embedded S parameters. As can be seen the series inductance over frequency does not change much with added pad parasitics.

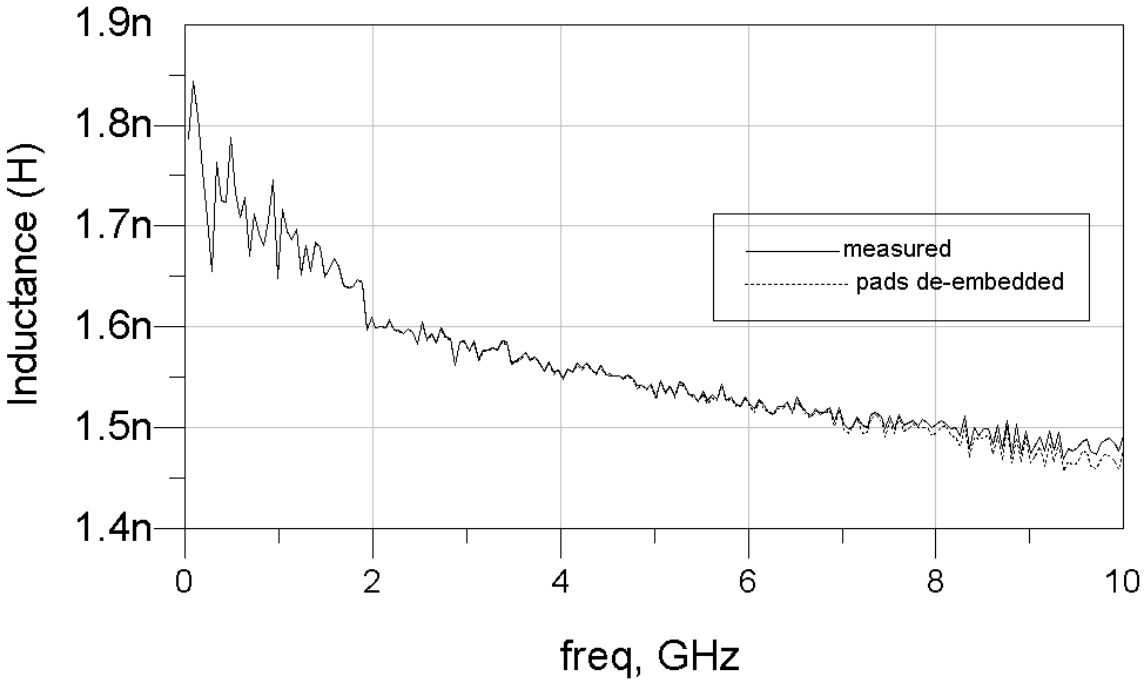

Fig. 14. Measured Series Inductance

Figure 15 shows the comparison of series inductance extracted from measured and simulated S parameter data from EM simulations. Both sets of data show the trend of decreasing inductance with frequency. The series inductance extracted from measured S parameters shows higher inductance value at lower frequencies and a steeper slope over the frequency range that is not predicted by the EM simulation. This decreasing inductance trend is attributed to the coupling between the metal spiral and the silicon substrate. The EM simulator does not completely model this effect at lower frequencies and therefore the slope of the simulated data is not that steep.

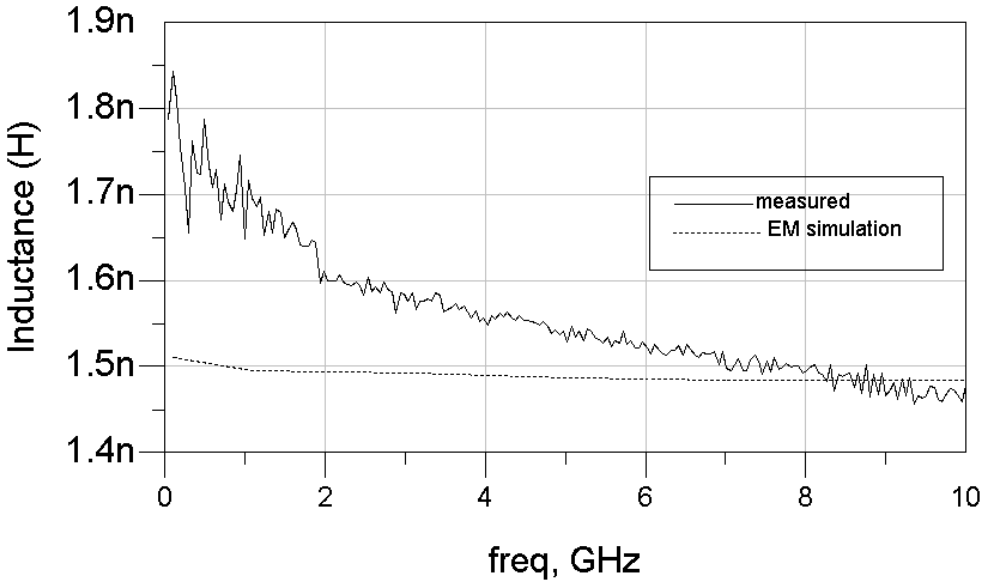

Fig. 15. Measured and Simulated Series Inductance

The above plots show that the EM simulator IE3D can be used as a tool to accurately simulate the frequency response of a given spiral inductor for a given process. The inductance results are accurate to within 0.3 nH. Accurate simulation results imply that an accurate scalable circuit model for the inductor that can be used in circuit simulations can be extracted using S parameter data from EM simulations.

3.5 Inductor Model

A lot of literature exists on accurate measurement and modeling of spiral inductors [4-11]. The model presented in Yue *et al* is commonly used to model spiral inductors [9]. Figure 16a shows 3-D view of the structure and 16b shows a schematic of the circuit model [9]. L_s and R_s represent the series inductance and series resistance of the spiral. C_s models the parasitic capacitance between the input and output ports of the inductor that allows the signal to flow from input to output without passing through the inductor. C_{ox} models the capacitance between the inductor and the substrate, and C_{si} and R_{si} model the capacitance and resistance of the silicon substrate [9]. Inductance is calculated using the concept of self-inductance of a wire and mutual inductance between a pair of wires. The mutual inductance between two wire segments is a function of the geometric mean distance between the wires, which in turn is a function of the wire width and pitch [9]. Most electro-magnetic simulators use Greenhouse's model to compute the series inductance of a circuit model given the geometry of the spiral. The Greenhouse model states that the overall inductance of a planar spiral is the sum of the self - inductance of each spiral segment and the positive and negative mutual inductances between all possible segment pairs. The series resistance R_s is a product of the skin effect and can be calculated using the closed form expression given in [9].

$$R = \frac{\rho . l}{\omega . t_{eff}} \qquad (3)$$

where ρ is the resistivity of the metal, l is the length of the metal, and t_{eff} is the effective thickness and is a function of the skin depth. As skin depth decreases with frequency, R_s increases [9]. C_s models the signal flow from input to output without flowing through the inductor. C_s can be expressed in a close form expression as in (4).

$$C_s = n * w^2 * \frac{\varepsilon_{ox}}{t_{oxM1-M2}} \qquad (4)$$

where n is the number of overlap, w is the width of the spiral and$t_{oxM1\text{-}M2}$ is the oxide thickness between the spiral and underpass. C_{ox} represents the oxide capacitance, while C_{si} and R_{si} represent the silicon capacitance and resistance respectively. R_{si} is determined mostly by the majority carrier concentration. C_{si} models the high frequency capacitive effects that originate in the semiconductor material. The parasitics can be expressed in close form as:

$$C_{ox} = \frac{1}{2} * l * w * \frac{\varepsilon_{ox}}{t_{ox}} \qquad (5)$$

$$C_{si} = \frac{1}{2} * l * w * C_{sub} \qquad (6)$$

$$R_{si} = \frac{2}{l * w * G_{sub}} \qquad (7)$$

where C_{sub} and G_{sub} are the capacitance and conductance per unit area for the silicon substrate. ε_{ox} and t_{ox} are the dielectric constant and thickness of the oxide layer between the inductor and the substrate.

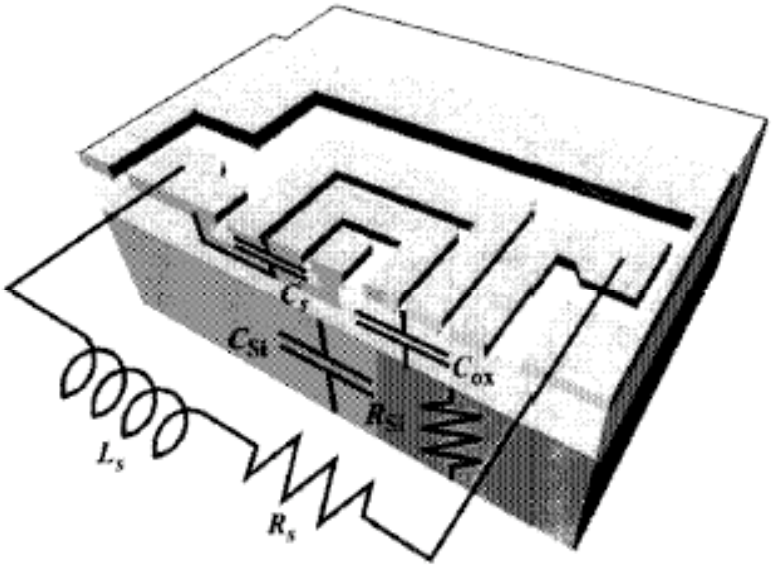

Fig. 16a. 3-D view of spiral structure

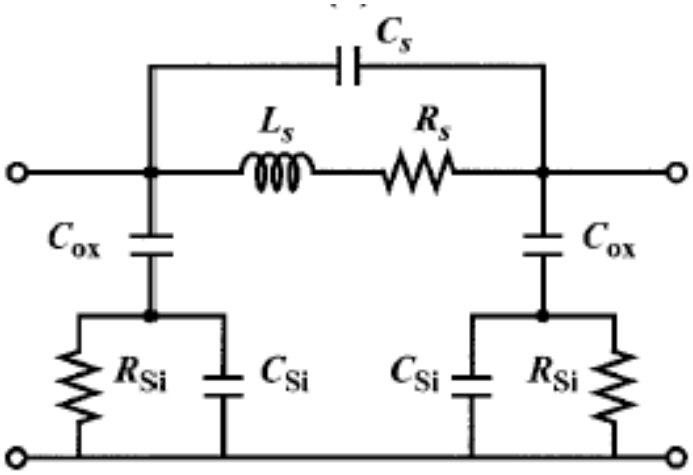

Fig. 16b. Circuit schematic of inductor pi model

3.6 Modified Inductor Model

In order to use the inductor in integrated circuits, an accurate and robust circuit model is required. The 9-element pi model described in the previous section has been used for spiral inductors on low-loss substrates such as high-resistivity silicon (HRS) or sapphire. However, this model does not accurately account for the eddy-current losses in the silicon substrate of medium to highly doped silicon processes. In such processes the series resistance and inductance exhibit a significant dependence on frequency [10]. The eddy-current loss in the substrate causes L(w) to decrease with increasing frequency and R(w) to increase with increasing frequency. The measurement results presented in the previous sections also show decreasing series inductance and increasing series resistance. The 9-element model exhibits an increasing inductance and resistance with frequency. In order to correctly model the decreasing inductance, the coupling capacitor C_s has been removed and a transformer loop has been added to account for the frequency dependent loss in the inductance. The initial element values are obtained using the closed form equations (3-7) and then optimized for matching to measurement results. Fig. 17 shows the modified model extracted for the structure fabricated. The mutual inductance M_s can be thought to represent the inductive coupling between the spiral metallization and the semi-conducting substrate. Figures 18a and 18b compare the measured and modeled frequency response of the spiral inductor. Figure 19 compares the measured inductance and the modeled inductance. Figure 20 compares the measures series resistance and the modeled series resistance. These results are for the spiral inductor structure alone without the effect of pad parasitics. Table 1 lists the element values for the circuit model presented.

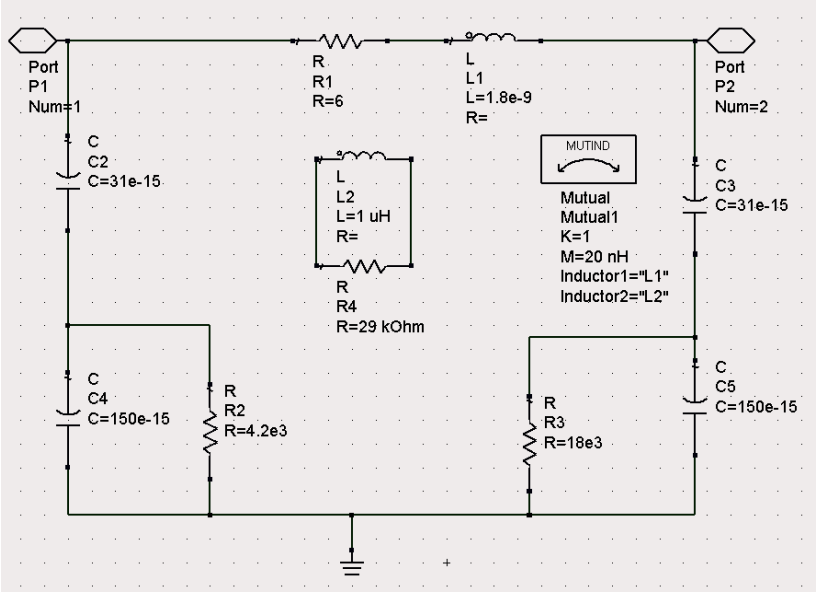

Fig.1 7. Schematic of inductor empirical model

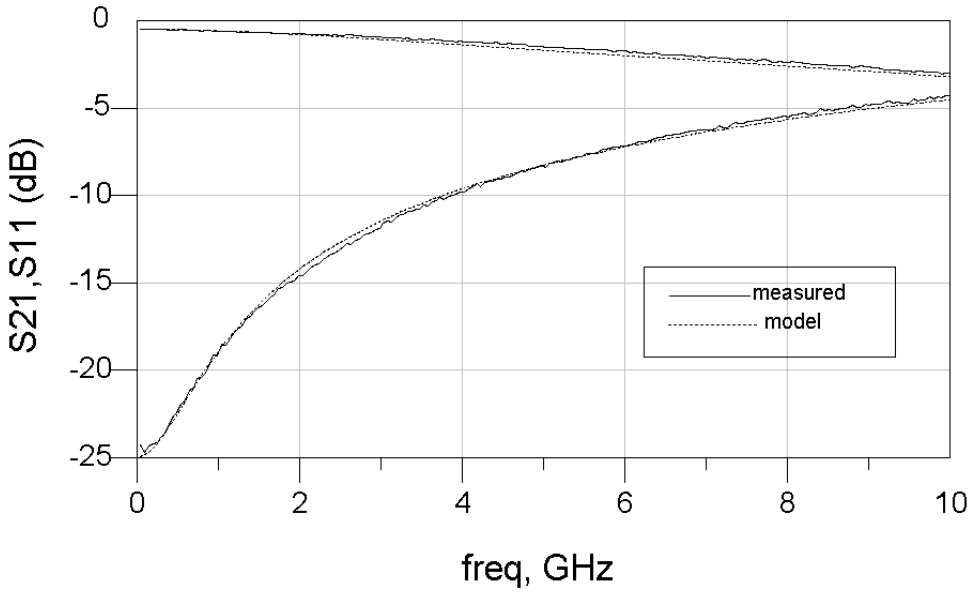

Fig. 18a. Frequency response of inductor model

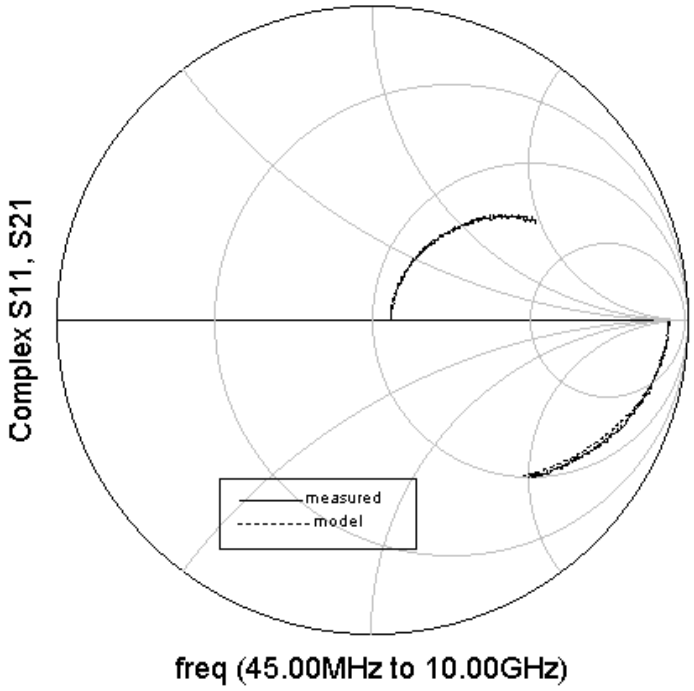

Fig. 18b. Frequency response of model in Smith chart format

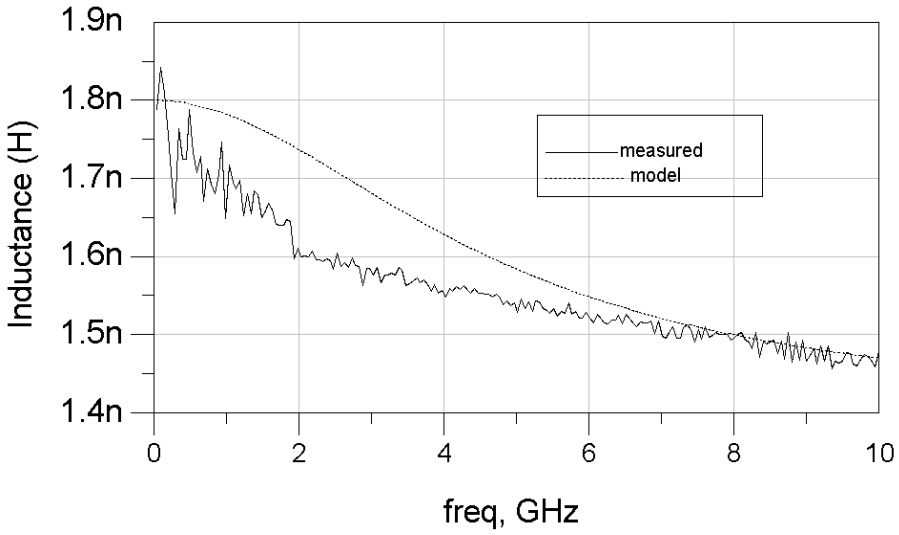

Fig. 19. L(w)

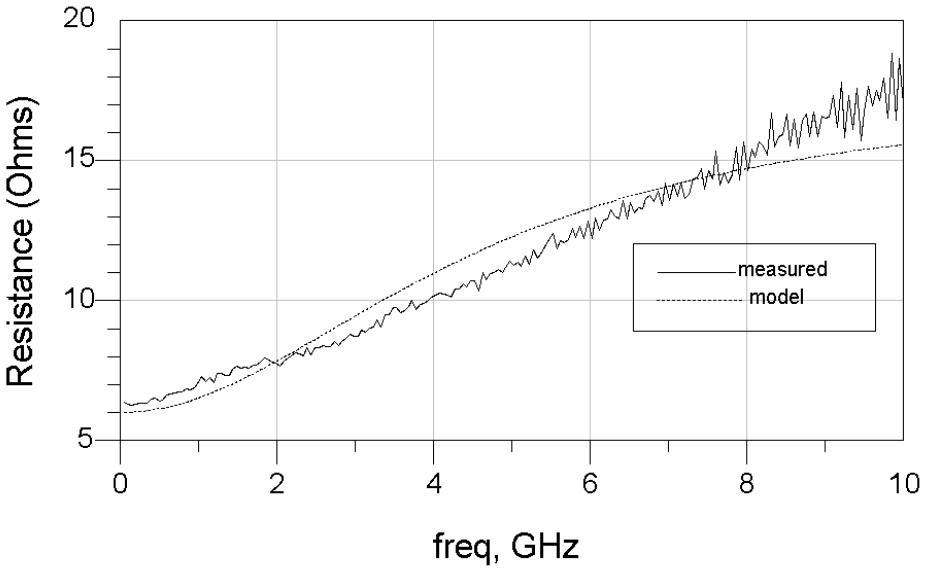

Fig. 20. R(w)

Table 1. Element Values for Inductor Model

Parameters	Value
R_{dc}	6 Ohm
L_{dc}	1.8 e-9
R_s	29 kOhm
L_s	1 uH
M_s	20 nH
C_{ox1}	31 fF
C_{ox2}	31 fF
R_{sub1}	4.2e3 Ohm
R_{sub2}	18e3 Ohm
C_{sub1}	150 fF
C_{sub2}	150 fF

CHAPTER 4

PASSIVE DELAY LINE

4.1 Delay Elements

As described in Chapter 2, a Feed-Forward Equalizer (FFE) is selected to equalize a 4 PAM signal after transmission through a 20-inch backplane channel. The FFE consists of gain blocks and delay elements. For such a high-speed application, accurate performance of the delay element becomes a critical factor in system performance. The delay line structure should be integrated with the rest of the circuit. Hence, it needs to be implemented on-chip. Furthermore, the delay element should be linear and wideband and not introduce any distortion in the signal. Since the overall system is differential and the equalizer circuit will take in a differential 4 PAM signal, the delay line is also required to be differential. To summarize, the system requires an integrated delay line structure to provide accurate delay to a high-speed differential signal. A passive delay line has the advantage of showing less sensitivity to supply voltage, temperature. Previous work has shown integrated passive delay lines in CMOS and SiGe [14,15].

4.2 Passive Delay Lines

As described in Chapter 2, LC ladder filters that have a linear phase response can provide time delay. Since, $t_d = -\frac{d(\arg(H(jw))}{dw}$, a linear phase response over the entire bandwidth results in constant group delay over the bandwidth. The best- known time delay filters are the Bessel –Thomson filters [3]. These filters have a maximally flat delay response. However, these filters are result in component values that are unrealistic for integration and are therefore not commonly used. Constant-k LC ladder networks have been used as delay elements [14,15]. Figure 21 shows a schematic of such a structure. The structure consists of identical inductors and capacitors in a ladder, resulting in a lumped approximation of a transmission line. The delay line takes in a differential signal and outputs a differential signal delayed by the designed delay value.

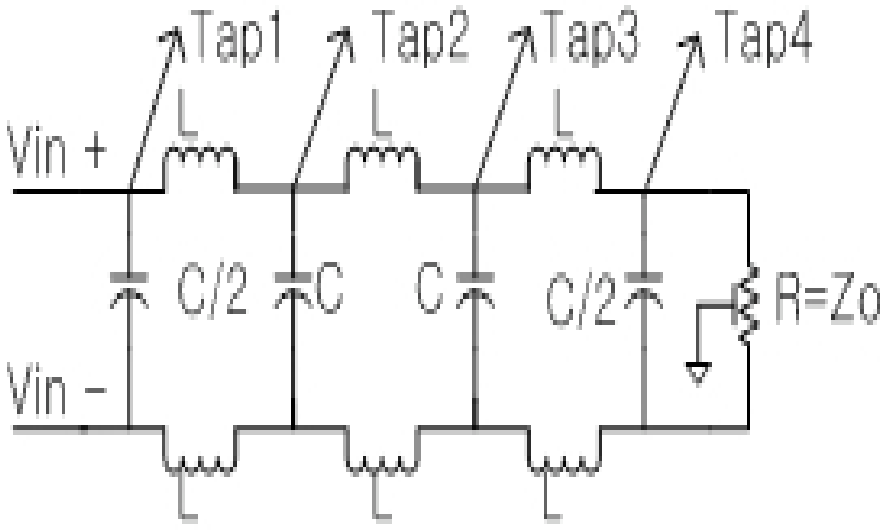

Fig. 21 Schematic of lumped element passive delay line

4.3 Calculations of L and C values.

From artificial transmission line theory, the following equations are valid to obtain L and C values for a delay line [3].

$$T_d = \sqrt{L_t C_t} \qquad \text{and} \qquad Z_o = \sqrt{\frac{L_t}{C_t}} \tag{8}$$

where T_d is the delay per section, and Z_o is the characteristic impedance of the artificial transmission line. In Figure 22, $L=L_t$ and $C=C_t/2$. As mentioned in Chapter 2, the required time delay after each tap is 33 picoseconds resulting in a total time delay of 99 picoseconds from input to output. The terminating and characteristic impedance of the structure is 50 Ohms. Knowing this, the L and C values for the delay line can be calculated. For a stand alone delay line with ideal inductors and capacitors, L_t=1.65 nH and C_t=660 fF.

In order to design an integrated FFE, an accurate circuit representation of the delay line is required. The inductor circuit model developed in Chapter 3 is used for circuit simulations. Taking into account transistor gate parasitics and other circuit parasitics, the delay line is designed to be integrated into the equalizer circuit and the capacitor values are adjusted for optimal system performance. Figure 22 shows the simulated frequency response of the delay line using the inductor model. Figure 23 shows the simulated group delay of the delay line having a total delay of 33 picoseconds *3 = 99 picoseconds.

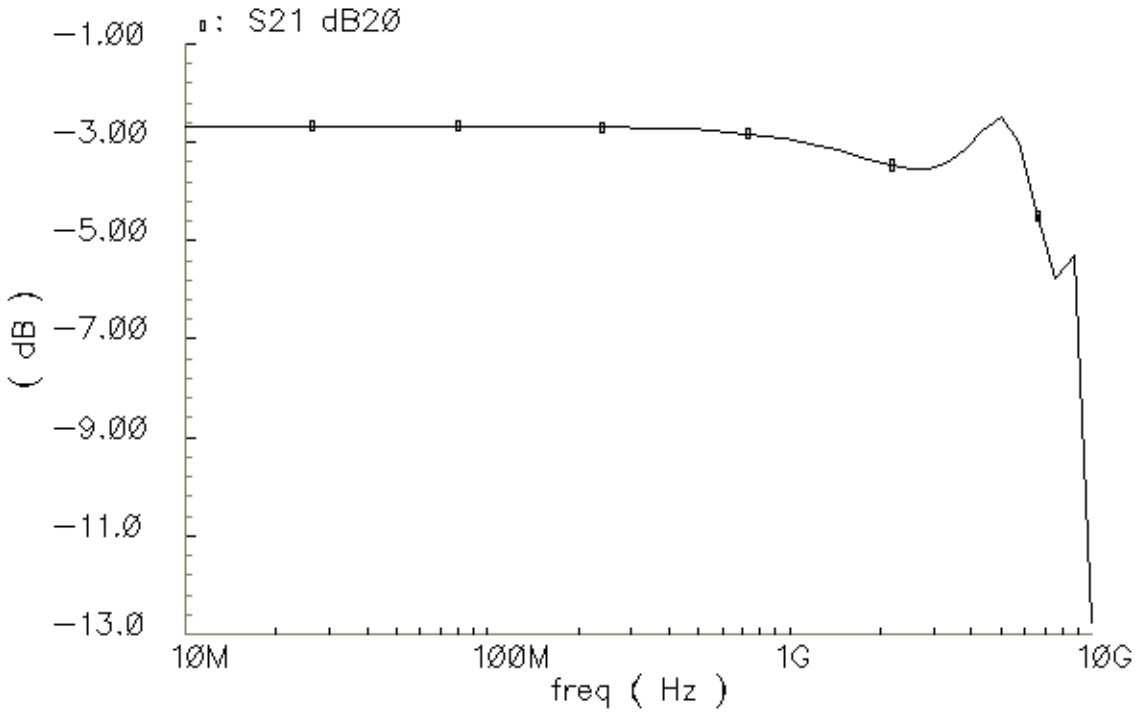

Fig. 22. Simulated Frequency response of delay line

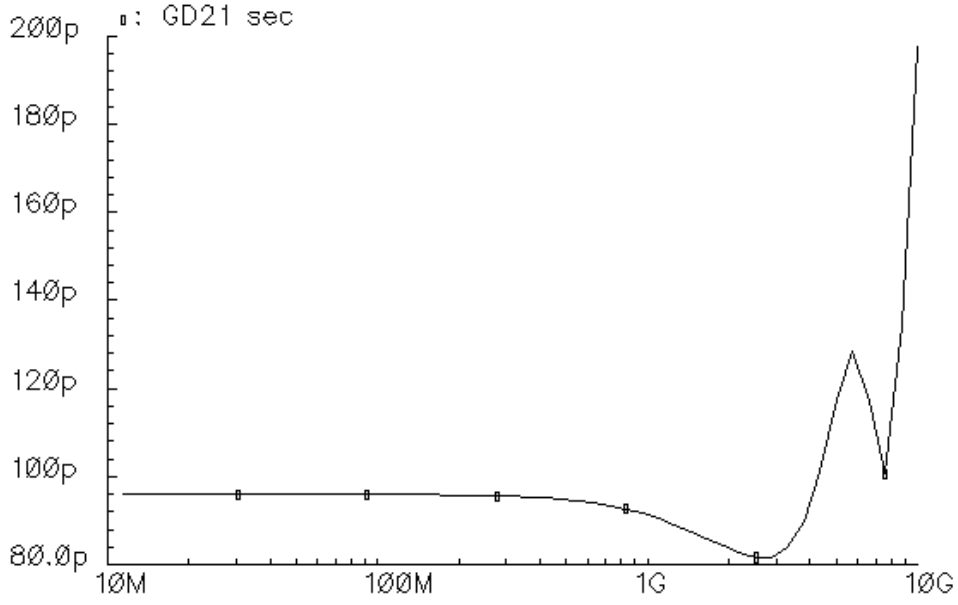

Fig. 23. Simulated group delay of delay line

4.4 Measurement Results

The delay line is fabricated using National Semiconductor's 0.18 um CMOS process. Figure 24 shows a die photo of the structure fabricated. The input and output signals are differential and have a GSSG pad configuration for measurement purposes. The chip was measured using Cascade Microtech's GSSG probes. In order to test the performance and signal integrity of the delay line, a 10 Gb/s PRBS 2^{23}-1 differential signal was transmitted through the delay line. The signal was generated using a Bit-Error-Rate Tester (BERT) and the output signal was received using a digital sampling oscilloscope. Figure 25 shows the eye diagram of a 10 Gb/s OOK signal. The delay line was also tested for 4-PAM transmission using a BERT. The 4-PAM signal was generated by combining two10 Gbp/s synchronous PRBS binary data using a power combiner and setting a delay between the two data streams. Figure 26a shows a 10 GSym/s 4 PAM signal sent as input to the delay line. This signal has a 20 Gbp/s data throughput. As can be seen, the input eye itself is not very clean. This is due to the limitations of the measurement setup, cables and connectors. The eye output from the delay line is measured using an oscilloscope. Fig. 26b shows the output eye at 8 GSym/s. Beyond this data rate, signal integrity was affected due to the quality of the input eye.

In order to measure the frequency response and the group delay of the delay line, the S parameters of the delay line were measured using the Agilent 4 port Vector Network Analyzer. As seen in Figure 27, the 3 dB bandwidth of the delay line is 5 GHz. Figure 28 shows the group delay of the passive delay line. The deviation from the design goal of 99 picoseconds is attributed to the system group delay extraction technique

because the delay as measured as part of the equalizer shown in Figures 30a-c show that each delay segment has about 33 picoseconds of delay.

The delay line was also fabricated as part of the FFE in the same process. Figure 29 shows the die photo of the FFE. The delay at each tap was measured by turning each successive tap on and all other taps off and sending a pulse through the FFE. Figures 30a, 30b, 30c show the delay after each tap. Each delay is close to the design value of 33 ps. This shows that the delay line as part of the FFE is able to provide accurate delay to the input signal at each tap.

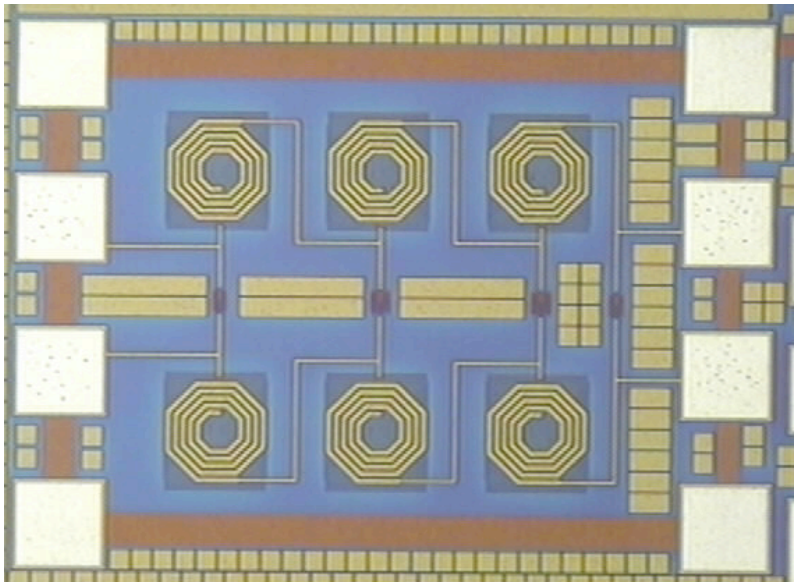

Fig. 24. Die photo of passive delay line

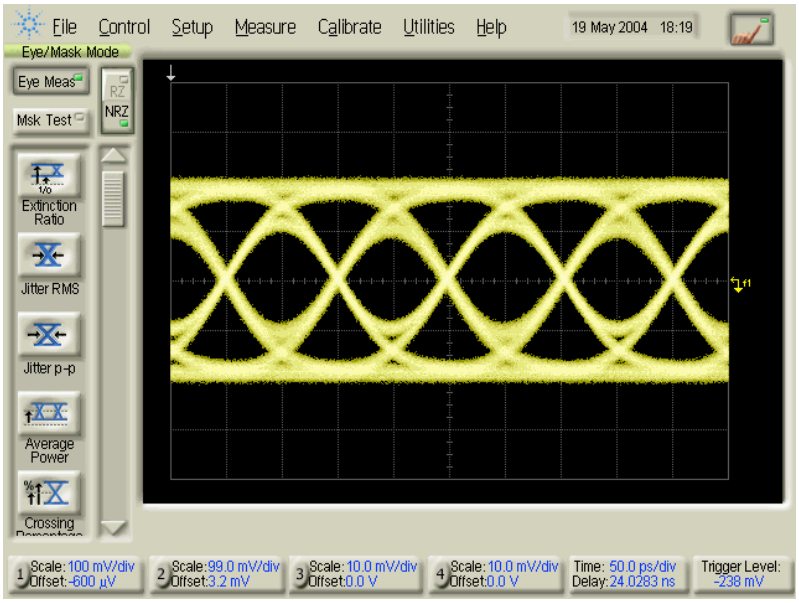

Fig. 25. Eye diagram of 10 Gb/s OOK signal through delay line

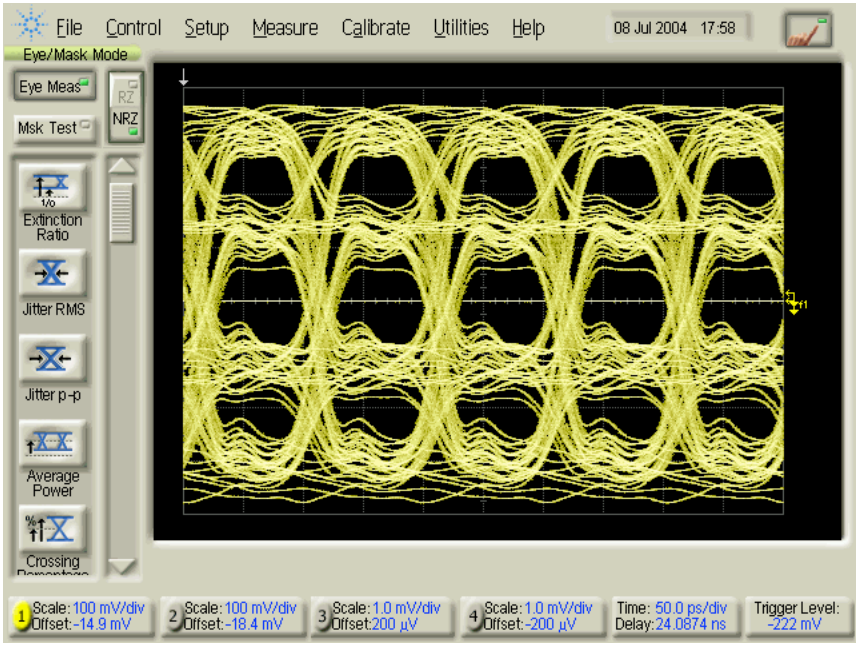

Fig. 26a. 10 GSym/s 4 PAM eye into the delay line

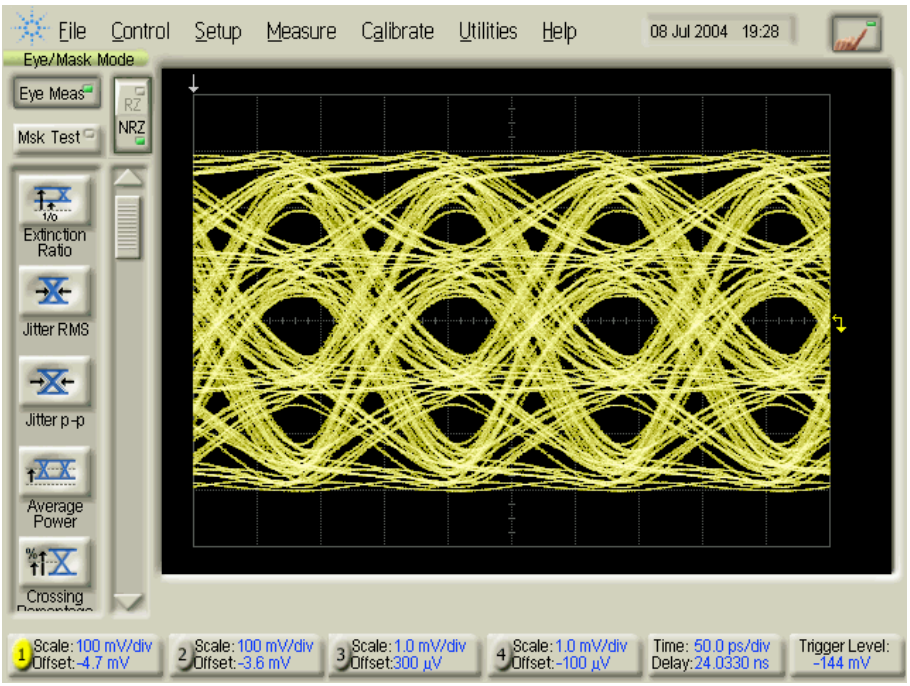

Fig. 26b. 8 GSym/s 4 PAM eye from delay line output

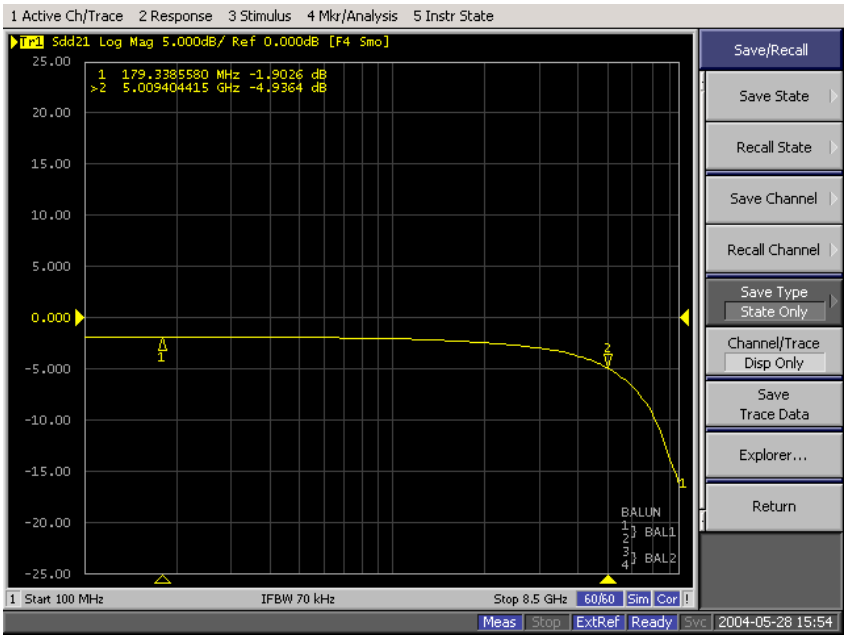

Fig. 27. Frequency response of the passive delay line

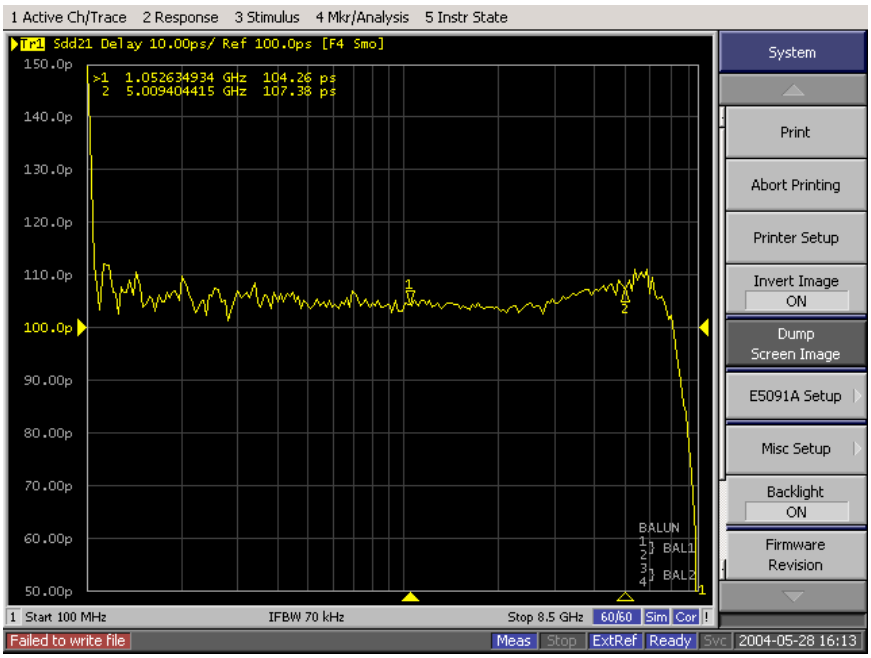

Fig. 28. Group Delay of passive delay line

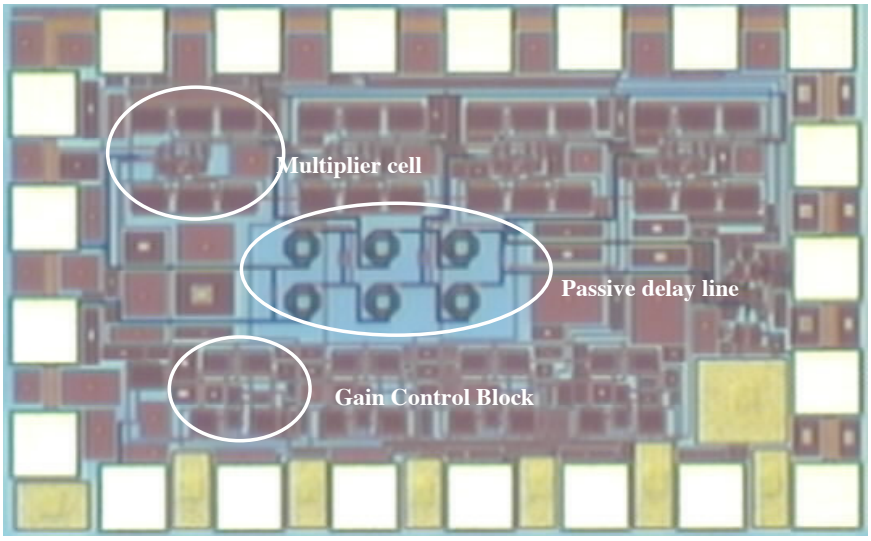

Fig. 29 Die photo of FFE

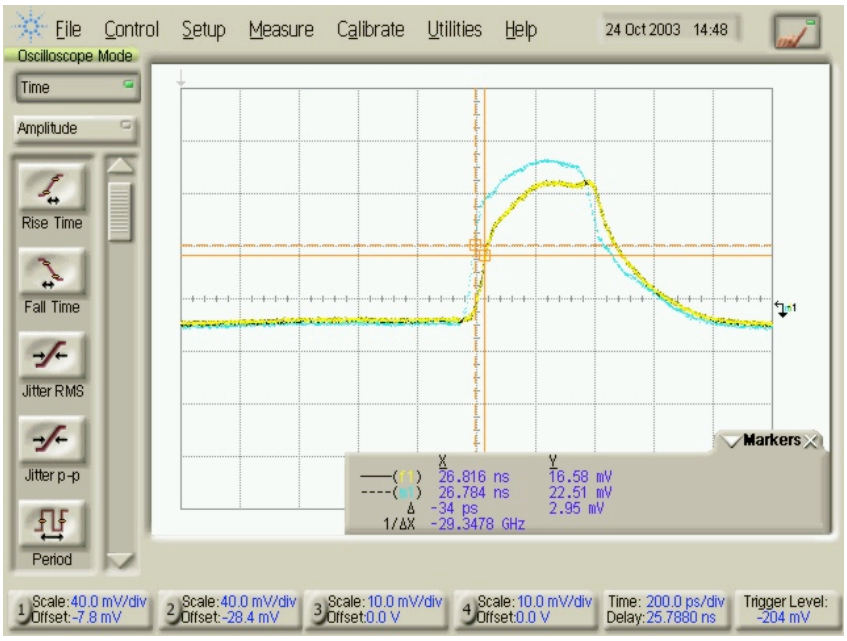

Fig. 30a. Delay between tap 1 and tap 2

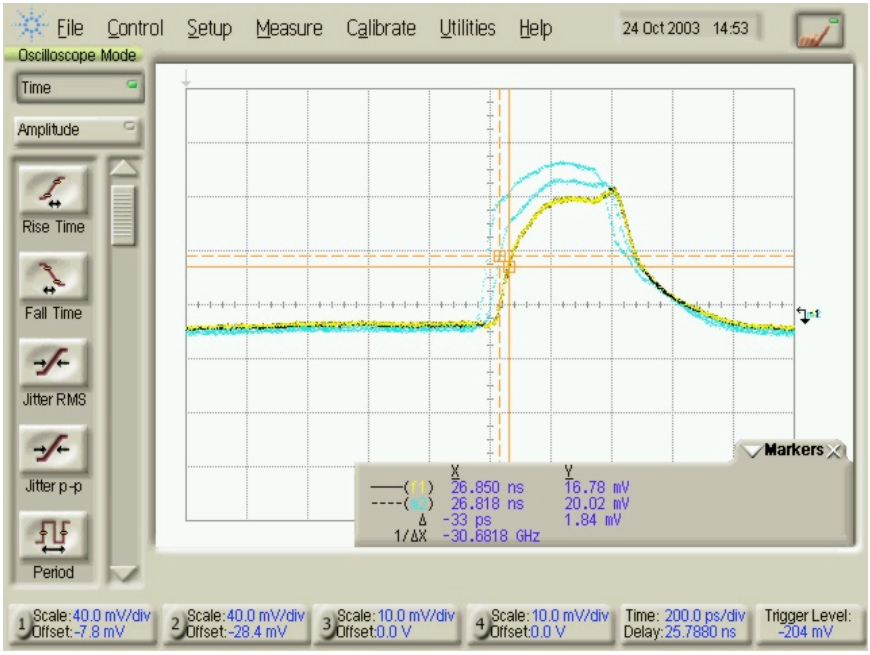

Fig. 30b. Delay between tap 2 and tap 3

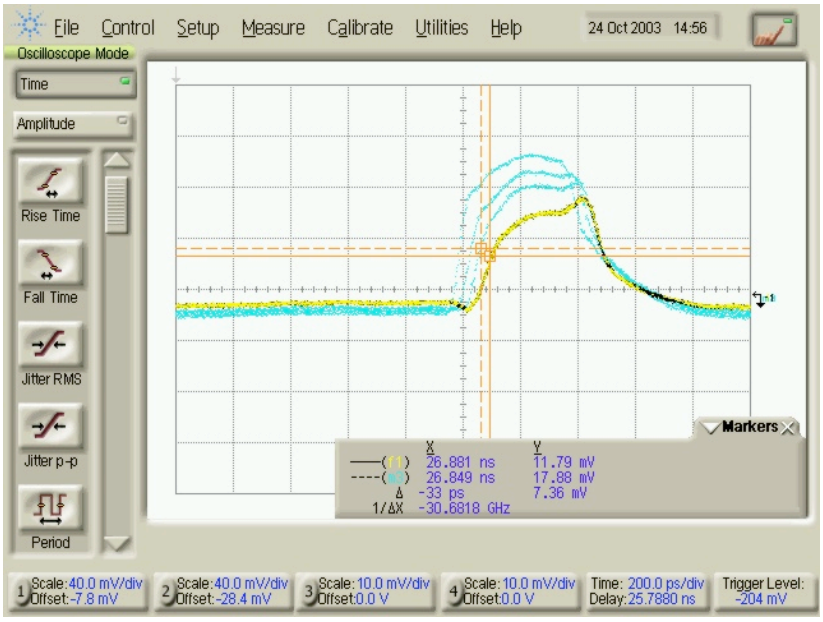

Fig. 30c. Delay between tap 3 and tap 4

The above plots show the performance of the delay line with respect to its application in a passive equalizer. Figures 24 and 25b show the signal integrity with a 10 GSym/s data throughput. This shows that the passive delay line should not compromise the signal integrity of the FFE when integrated. Figure 27 illustrates the bandwidth of the passive delay line structure. Figures 30a-c illustrate the accuracy of the time delay structure. These results show that the passive delay line structure can be integrated as part of an FFE to provide accurate time delay at each tap. Chapter 5 will conclude with a summary and recommendations for future work.

CHAPTER 5

CONCLUSION

5.1 Summary and Evaluation

A passive delay line structure implemented in a 0.18 um CMOS process for use in a Feed-Forward-Equalizer (FFE) has been demonstrated in this thesis. The delay line requires the use of wide-band inductors. The thesis demonstrates design, EM simulations, fabrication and measurement results of a wideband inductor used as part of the delay line. A lumped element model for the spiral inductor is also presented for use in circuit simulations. The thesis demonstrates the design procedure, fabrication and measurement results of the passive delay line structure showing performance at 10 Gb/s OOK and 8 GSym/s 4-PAM with 33 picoseconds of delay at each tap. This demonstrates that the wide band and accurate time delay structure can be integrated as part of a FFE in a 0.18 um CMOS process. To the author's knowledge, this is the first successful demonstration of a passive delay line implemented in CMOS and operating at these speeds.

5.2 Recommendations for Future Work

The core component of the passive delay line structure is the inductor. Accurate circuit simulations using the passive delay line require an accurate inductor circuit model operating over the entire bandwidth. The EM simulation tool has been shown to simulate spiral inductor performance in a given process. The EM simulations can be used to develop a scalable inductor model for a given process cutting down the design cycle time.

A thorough analysis of inductor design and modeling can be done using IE3D and similar tools to accurately model every parasitic effect of the fabricated spiral.

5.3 Conclusion

A passive delay line structure implemented in a 0.18 um CMOS process for use in a FFE has been demonstrated. The delay line has been shown to transmit a 10 GSym/s signal demonstrating its bandwidth capabilities and has been shown to provide accurate time delay to an input differential signal. To the author's knowledge, this is the first successful demonstration of a passive delay line implemented in CMOS and operating at these speeds.

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